SEMINAR ANNOUNCEMENT

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Area: Integrated Circuits & Embedded Systems

Host: Professor Alioto, Massimo Bruno

TOPIC	:	**Steep-slope and Dirac-source FETs for ultra-low-voltage and low-energy CMOS circuits**
SPEAKER	:	**Professor David Esseni** **University of Udine**
DATE	:	**Thursday, 19 Sep 2024**
TIME	:	**12.00PM to 1.00PM**
VENUE	:	**E7-03-09 - Seminar Room 4** **College of Design and Engineering, National University of Singapore**

ABSTRACT

In a foreseeable future, nanoelectronics will deliver energy autonomous sensing, computing and communicating devices for countless applications. As of today, however, power consumption is one of the main impediments to the implementation of such scenarios, and CMOS technologies have entered a new era where energy efficiency is a paramount figure of merit. The importance of energy efficiency has been further emphasized by the fact that CMOS technologies are the hardware backbone for the explosion of AI applications.

In an attempt to aggressively reduce the supply voltage, VDD, new steep-slope transistor concepts and materials have been and are being investigated to achieve a room temperature subthreshold swing (SS) smaller than 60mV/dec (a fundamental limit of room-temperature operation of CMOS FETs).

In this seminar, I will first introduce the working principle of some steep-slope transistors (e.g. Tunnel FETs and Negative Capacitance FETs), and then focus on a novel and intriguing device concept known as Dirac Source FET (DSFET). In fact, Graphene (Gr) and Dirac semi-metals have a Density of States proportional to |E−ED| for an energy E close to the Dirac energy ED. Hence, in the source of a Dirac-Source FET (DSFET) the electron density n(E) decays more steeply than the tail of the Fermi-Dirac function, thus overcoming the Boltzmann tyranny and leading to a 60mV/dec operation in sub-threshold. Differently from Tunnel FETs, the sub-thermionic transport mechanism in DS-FETs does not rely on tunnelling, hence a large drive current has been singled out as a distinct advantage of this intriguing device concept.

BIOGRAPHY

David Esseni received the Laurea degree and the Ph.D. in Electronic Engineering from the University of Bologna. During year 2000 he was a visiting scientist at Bell Labs - Lucent Technologies, Murray Hill (NJ-USA) and during 2013 he was visiting professor at the University of Notre Dame (IN, USA). Since 2015 he has been Professor of Electronics at the University of Udine, Italy.

His research interests are mainly focused on the characterization, the modelling and the design of advanced MOS transistors and semiconductor non-volatile memories. D.Esseni is the author of about numerous papers in international journals and conferences, including more than 40 papers presented at IEDM. He is co-author of the book "Nanoscale MOS transistors: Semi-classical transport and application" (Cambridge University Press, Cambridge (UK), 2011) and of several book chapters devoted to different topics related to transport in nanoscale MOSFETs. From 2008 to 2017 D.Esseni was Editor of IEEE Transactions on Electron Devices (T-ED) and co-guest Editor of special issues published in IEEE TED and IEEE Journal of Electron Devices. D.Esseni has served or is serving as a member of the technical committee of the International Electron Devices Meeting (IEDM), the International Reliability Physics Symposium (IRPS), the European Solid-State Device Research Conference (ESSDERC) and the International Conference on Simulation of Semiconductors Processes and Devices (SISPAD). He was the Chairman of the SISPAD 2019 edition, which was held in Udine in September 2019. In 2012 D.Esseni was awarded a Fulbright Fellowship and spent six months as a Research Scholar at the University of Notre Dame (IN, USA). Since 2013 D.Esseni is a Fellow of the IEEE, EDS Society.

David Esseni was the PI or the PI for the University of Udine for several research projects funded either by Italian Ministry of Universit, by the European Community, or by industries.

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